Reg. No. | | | | | | | | |

G. VENKATASWAMY NAIDU COLLEGE (AUTONOMOUS), KOVILPATTI – 628 502.

UG DEGREE END SEMESTER EXAMINATIONS - APRIL 2025.

(For those admitted in June 2023 and later)

PROGRAMME AND BRANCH: B.Sc., ELECTRONICS

SEM	CATEGORY	COMPONENT	COURSE CODE	COURSE TITLE
II	PART-III	CORE-3	U23EL202	DIGITAL ELECTRONICS

Date & Session: 28.04.2025/FN **Time: 3 hours** **Maximum: 75 Marks**

Course Outcome	Bloom's K-level	Q. No.	SECTION – A (10 X 1 = 10 Marks) Answer ALL Questions.
CO1	K1	1.	Convert binary to octal: $(110110001010)_2$ =? a) $(5512)_8$ b) $(6612)_8$ c) $(4532)_8$ d) $(6745)_8$
CO1	K2	2.	What are the mantissa and exponent required respectively to represent '5' in binary floating point representation? a) 011,0.110000 b) 0.110000,011 c) 011,0.101000 d) 0.101000,011
CO2	K1	3.	Which of the following is an incorrect SOP expression? a) x+x.y b) (x+y)(x+z) c) x d) x+y
CO2	K2	4.	Identify, which of the following expression is output of Ex-OR gate? a) A'B+AB' b) AB+A'B' c) A+A.B d) A'+B'
CO3	K1	5.	A combinational circuit that selects one from many inputs are _____ a) Encoder b) Decoder c) Demultiplexer d) Multiplexer
CO3	K2	6.	Let A and B is the input of a subtractor then the difference output will be ___. a) A XOR B b) A AND B c) A OR B d) A EXNOR B
CO4	K1	7.	In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____ a) D flip-flop b) S-R flip-flop c) T flip-flop d) S-K flip-flop
CO4	K2	8.	Indicate the main difference between a register and a counter. a) A register has no specific sequence of states b) A counter has no specific sequence of states c) A register has capability to store one bit of information but counter has n-bit d) A register counts data
CO5	K1	9.	Which of the following has the lowest access time? a) RAM b) ROM c) Registers d) Flag
CO5	K2	10.	PLA contains _____ a) AND and OR arrays b) NAND and OR arrays c) NOT and AND arrays d) NOR and OR arrays

Course Outcome	Bloom's K-level	Q. No.	**SECTION – B (5 X 5 = 25 Marks)** **Answer ALL Questions choosing either (a) or (b)**
CO1	K3	11a.	Show the binary addition (-43) + (-78). **(OR)**
CO1	K3	11b.	Illustrate the ASCII code with an example.
CO2	K3	12a.	Simplify the expression Y= $\sum_m$ (7, 9, 11, 12, 13, 14, 15), using the K-map method. **(OR)**
CO2	K3	12b.	Explain the function of AND gate with neat diagram.
CO3	K4	13a.	Describe the working of a full-adder with neat logic circuit. **(OR)**
CO3	K4	13b.	Design a 1-to-4 demultiplexer and explain its operation.
CO4	K4	14a.	Describe the 4 bit serial-in-serial out shift register with neat logic diagram **(OR)**
CO4	K4	14b.	Compare shift register with counter.
CO5	K5	15a.	Explain the difference between RAM and ROM. **(OR)**
CO5	K5	15b.	Discuss the function of programmable array logic.

Course Outcome	Bloom's K-level	Q. No.	**SECTION – C (5 X 8 = 40 Marks)** **Answer ALL Questions choosing either (a) or (b)**
CO1	K3	16a.	Perform the following conversion (i). $(A6F)_{16}$ = ---------- ( )$_8$? (ii). $(127)_{10}$ = ---------- ( )$_2$? (iii). $(3764)_8$ = ---------- ( )$_{16}$? (iv). $(11101)_2$ = ---------- ( )$_{10}$? **(OR)**
CO1	K3	16b.	Briefly explain the Excess-3 code, Gray code.
CO2	K4	17a.	State Boolean laws and theorems. **(OR)**
CO2	K4	17b.	Explain how the basic gates can be realized using NOR and NAND gates.
CO3	K4	18a.	Show how a full adder can be converted to a full-subtractor with the addition of an inverter circuit.
CO3	K4	18b.	**(OR)** Illustrate the binary to gray and gray to binary code converter logic circuit.
CO4	K5	19a.	Explain the operation of J-K flip-flop and master-slave J-K flip-flop. **(OR)**
CO4	K5	19b.	Explain the working of 4-bit ring counter with neat logic circuit.
CO5	K5	20a.	Classify the different types of ROM and explain in detail. **(OR)**
CO5	K5	20b.	Discuss in detail about field programmable gate arrays.